**#11.7** “How many PCI-Express lanes are required to support a 10 gb per second Ethernet card?”

*Answer:*

4 pci-express lanes are requiring to support 10 gbps.

PCI-Express has essentially replaced an older bus, called simply PCI. PCI-Express is a serial I/O bus that was designed to replace the parallel PCI bus that long dominated backplane design. PCI-Express is designed to be data and signal compatible with components designed for the PCI bus. The original PCI bus was a “32- or 64-bit” (meaning 32 or 64 bits of data at a time) backplane bus that provided plug-in capability for various I/O modules that control external serial and parallel ports, sound cards, network cards, and the like.  
The PCI bus provided 32 or, optionally, 64 lines that were used for both addresses and data, labeled AD00 through AD31 or AD63, plus various control and power lines.

PCI is the one that determines the devices that are connected to the motherboard. In a single PCI slot, there are lanes such as 1, 4, 8, 16. Two unidirectional differential pairs are present in each lane. PCI 4.0/x4 can able to handle 7.88 gbps.

10 gbps = 10000/8 = 1250 mbps. The 4 lanes can be enough to support the card with 10 GB per second.

As described in the text, the PCI-Express bus consists of thirty-two “lanes “. As of January 2009, each lane is capable of the maximum data rate of 500 MB per second. Lanes are allocated to a device 1,2,3,8,16, or 32 lanes at a time.

Assume that a PCI-Express bus is to be connected to a high-definition video card that is supporting a 1920 x 1080 true color (3 bytes per pixel) progressive scan monitor with a refresh rate of 60 frames per second. How many lanes will this video card require to support the monitor at full capability?”

*Answer:*

0 lanes at full capacity

**Explanation:**

We have that 1 pixel = 3 bytes, we have 1920\*1080 pixels, in order to find the number of bytes we do the product

1920\*1080\*3 = 6220800 B or 6.221MB.

We have that the monitor refreshes 60 times per second! let's multiply that number by 60

1920\*1080\*3\*60 = 373248000 [B/second] or 373.2 [MB/second]

Therefore, we are not using a single lane at its full capacity (500 MB/S), all the information could be carried out by a single lane.

Reference:  Englander, I. (2014). The \*architecture of computer hardware, systems software, and networking: An information technology approach: An information technology approach. In The \*architecture of computer hardware, systems software, and networking: An information technology approach: An information technology approach (pp. 342-343). Hoboken: Wiley.